REMARKS

The Office Action dated January 22, 2007 has been received and carefully noted. The the following remarks, are submitted as a full and complete response thereto.

Claims 1-60 are respectfully submitted for consideration.

The Office Action rejected claims 1-60 under 35 U.S.C. 103(a) as being obvious over US Patent NO. 6,021,132 to Muller et al. (Muller), in view of US Patent No. 6,529,519 to Steiner et al. (Steiner), in further view of US Patent No. 6,427,185 to Ryals et al. (Ryals). The Office Action took the position that Muller disclosed all of the features of these claims except a single buffer per packet mechanism or an index key. The Office Action asserted that Steiner and Ryals disclosed these features respectively. Applicants submit that the cited references taken individually or in combination, fail to disclose or suggest all of the features of any of the pending claims.

Claim 1, from which claims 2-7 depend, is directed to a memory structure. An Address Resolution Table resolves addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address. A Packet Storage Table, is adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table. A single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access

in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 8, from which claims 9-12 depend, is directed to a memory structure. An Address Resolution Table having an associative memory structure uses a key to index a location within the Address Resolution Table. The Address Resolution Table resolves addresses in a packet-based network switch. A single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The key is a predefined portion of a packet destination address.

Claim 13, from which claims 14-27 depend, is directed to a memory structure having a memory block. The memory structure includes an Address Resolution Table having an associative memory structure. The Address Resolution Table resolves addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table. A Transmit Descriptor Table is associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value. The Packet Storage Table is adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a

single access in order to locate an entire packet at the location using the key wherein the key is a predefined portion of a packet destination address.

Claim 28, from which claims 29-31 depend, is directed to a packet-based switch. The packet-based switch includes a shared memory structure having an Address Resolution Table and a Packet Storage Table. A key indexes a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address. A single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 32, from which claims 33-51 depend, includes some of the features of claim 13, but is drawn to a packet-based switch.

Claim 52, from which claims 53-56 depend, includes some of the features of claim 8, but is drawn to a packet-based switch.

Claim 57, from which claims 58-60 depend, includes some of the features of claim 8, but is drawn to a packet-based switch.

Applicants respectfully submit that each of the above claims recites features that are neither disclosed nor suggested in the cited references.

Muller is directed to shared memory management in a switch network element. Muller describes a shared memory manager 220 that is exploited by input and output ports 206 by locally storing pointers to buffers that contain packet data rather than locally

storing the packet data. A predetermined number of buffer pointers are kept on hand to allow immediate storage of received packet data. The buffer pointers are preallocated during the initialization of switching element 100 and requested from shared memory manager 220. Pointers are queued to buffers that contain packet data, and not to the packet data itself. Further, a packet can be stored over more than one buffer. Each buffer in shared memory 230 is owned by one or more different ports at different points in time without having to duplicate the packet data.

Steiner is directed to prioritized-buffer management for fixed size packets in a multimedia application. Steiner describes a memory system that includes a tag register for storing tags associated with respective pages, wherein each tag indicates whether the associated page is empty or full. Steiner also describes a shadow register for storing conflict-free updates from the tag register and a page register for storing pointers to the lowest free or unoccupied page. Steiner also describes a buffer that is organized along packet boundaries or pages for convenience of operation. A processor maintains a table of pointers to each packet boundary, and, therefore, knows the location of all leftover packets. A tag register 40 is provided, that has as many bits as there are packet boundaries of buffer 22.

Ryals is directed to a switching device includes network interface cards connected to a common backplane. Each interface card is configured to support the maximum transfer rate of the backplane by maintaining a "pending" queue to track data that has been received but for which the appropriate routing destination has not yet been

determined. The switching device includes a switch controller that maintains a central card/port-to-address table. When an interface card receives data with a destination address that is not known to the interface card, the interface card performs a direct memory access over a bus that is separate from the backplane to read routing data directly from the central table in the switch controller. Each interface card builds and maintains a routing information table in its own local memory that only includes routing information for the destination addresses that the interface card is most likely to receive.

Applicants respectfully submit that the cited references, taken individually or in combination, fail to disclose or suggest all of the features of the above claims because Ryals fails to cure the admitted deficiencies of Muller and Steiner for the reasons set forth below.

Specifically, the cited combination of references fail to disclose or suggest at least the feature of an Address Resolution Table for resolving addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address, as recited in claims 1, 8, 13, 28, 32, 52 and 57. The Office Action alleged that Ryals cured these deficiencies in col. 9 line 15- col. 10 line 17.

However, Ryals merely discloses interface cards adding entries to their local tables. A table entry contains the pointer to the cell slot and the destination address contained in the cell is place on the pending queue. See col. 9 lines 15-20. However Ryals is silent with regards to a key being a predefined portion of the destination address.

Ryals at best describes that the entire destination address is entered into the table. Thus, Ryals fails to cure the admitted deficiencies of Muller and Steiner.

Applicants respectfully submit that because claims 2-7, 9-12, 14-27, 29-31, 33, 51, 53-56 and 58-60 depend from claims 1, 8, 13, 28, 32, 52 and 57, these claims are allowable at least for the same reasons as claims 1, 8, 13, 28, 32, 52 and 57, as well as for the additional features recited in these dependent claims.

Based at least on the above, Applicants respectfully submit that the cited references, taken individually or in combination, fail to disclose or suggest all of the features recited in claims 1-60. Accordingly, withdrawal of the rejection under 35 U.S.C. 103(a) is respectfully requested.

Applicants respectfully request that each of claims 1-60 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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Enclosures: Petition for Extension of Time
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